*ФИЗИКА ЭЛЕМЕНТАРНЫХ ЧАСТИЦ И АТОМНОГО ЯДРА*
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# DIGITAL OPTICAL MODULE ELECTRONICS OF KM3NeT

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The KM3NeT neutrino telescope is being built in the Mediterranean Sea and, once completed, it will be composed by tens of thousands of glass spheres (nodes), each including 31 small photocathodes (3″). The readout and data acquisition system of KM3NeT has to collect, treat, and send to the shore, in an economic way, the enormous amount of data produced by the photomultipliers and, at the same time, to provide time synchronization between each node at the level of 1 ns. The present paper describes all the electronics developed for achieving this goal.

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## INTRODUCTION

KM3NeT is a future European research facility in the Mediterranean Sea which will house a neutrino telescope of cubic kilometer scale. Cherenkov light from neutrino-induced secondary particles will be detected by an array of optical modules consisting of high-pressure resistant glass vessels with photomultipliers inside. This vessel is called the Digital Optical Module (DOM) and it is composed of 31 small 3-inch PMTs distributed around the glass sphere, which collects the Cherenkov light and transforms it into electronic signals [1, 2]. Figure 1 shows the Digital Optical Module and the KM3NeT overview.

The PMTs are suspended in a foam support structure: 19 in the lower hemisphere and 12 in the upper hemisphere. Each PMT has its own adjustable high-voltage supply integrated in the PMT base. The PMTs collect the Cherenkov light and convert it into electronic signals [3]. In order to translate these signals into the arrival time of the photons, they are processed by Time to Digital Converters (TDCs) core embedded in the Field Programmable Gate Array (FPGA) of the Central Logic Board (CLB). The CLB integrates the White Rabbit Protocol,

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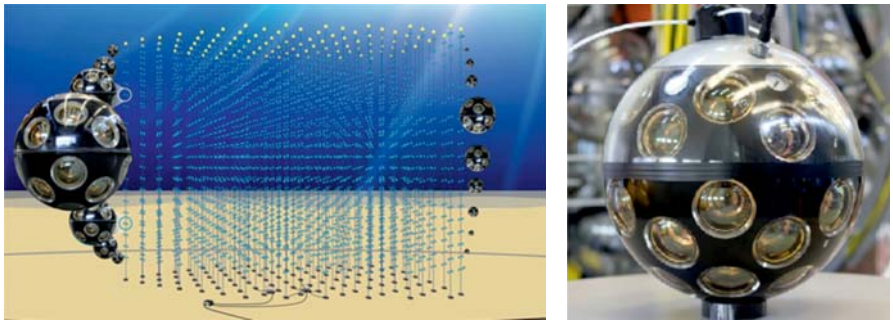

Fig. 1. KM3NeT general overview (left), Digital Optical Module (right)

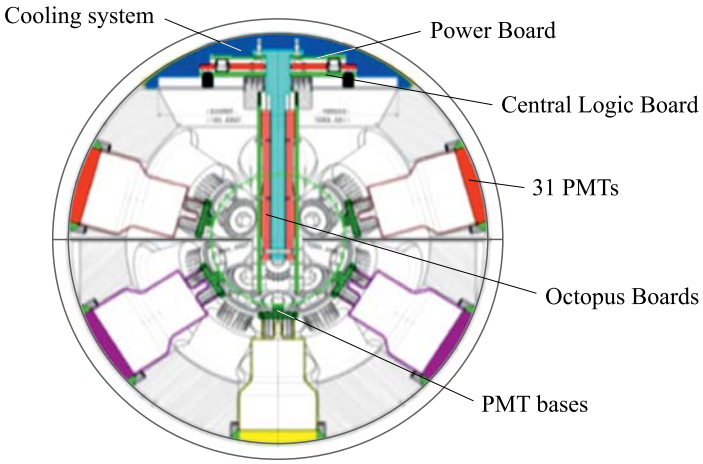


Fig. 2. DOM: position of the Power Board, Central Logic Board, Octopus Board, and PMT bases

a fully deterministic Ethernet-based network for general-purpose data transfer and synchronization, that allows one to synchronize all the KM3NeT DOMs with 1-ns resolution. The data provided by the PMT bases are collected and distributed to the CLB by means of two boards (one for each hemisphere), the so-called Octopus Boards. It also contains the electronic and photonic components for an optical serial link to the shore. All necessary DC power is provided by the Power Board (PB). An aluminium structure provides heat conduction between the electronics inside and the exterior of the sphere [4]. In Fig. 2, a schematic view of the DOM is shown.

## 1. PHOTOMULTIPLIER BASE

The PMT base is in charge of discretizing the signal read by the PMT and providing the High Voltage (HV) for the PMT. The PCB contains a preamplifier, a comparator (Time Over Threshold), and an identifier module. Connection to the PMT is done by flying leads with a PCB that has a diameter of 38 mm. Every PMT must give the same output signal when it is hit by a single photon. The gain of a PMT depends on the supplied high voltage. The HV for each PMT is individually adjustable from 800 to 1400 V. Consequently, each PMT gets its own HV circuit board. $I^2C$ protocol is used to be able to program the PMT base and to change the HV. The power consumption of each PMT base is around 4.5 mW. An additional function of the PMT base is the digitization of the analog output signal of the PMT. The output signal is converted from a charge signal to a voltage signal, followed by a conversion to a digital level by a comparator, resulting in a Time Over Threshold (TOT) signal. The comparator can be adjusted to the required TOT value using $I^2C$ protocol. The TOT signal is transferred to the DOM logic by an LVDS connection. To identify the PMT base, an ID circuit is added. The analog and digital signal conversion functionality of the PMT base is performed in an ASIC. The PMT base diagram is shown in Fig. 3.

**PMT Base ASIC.** The DOM is very crowded and there is little available space for the 31 PMTs and the PMT bases. In order to minimize space, cost, and power, an ASIC has been designed to read out the PMT. The PMT base houses the PROMiS ASIC. The Cockroft–Walton HV supply circuit on the base

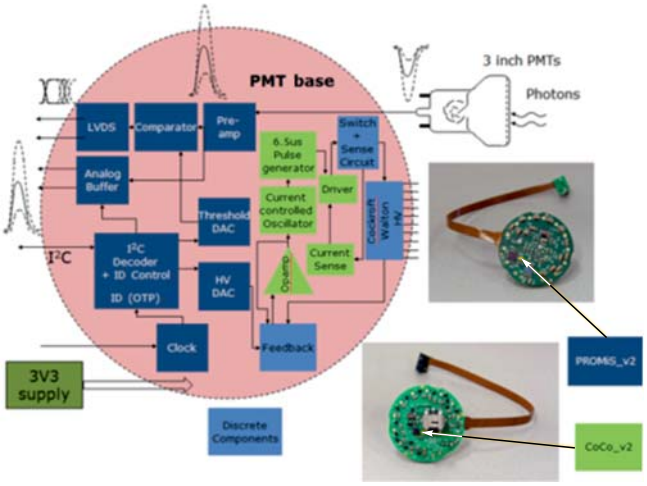


Fig. 3. PMT bases diagram

*Table* 1. **Specifications of PROMiS chip**

| | |
|---|---|
| Time resolution (for a single photon, photomultiplier + electronics), ns | $< 2$ |
| Two-hit time separation, ns | $< 25$ |
| Power consumption, mW | 35 |
| Supply voltage, technology | 3.3 V, 0.35 $\mu$ CMOS AMS |
| Comparator Threshold Adjustment | 8 bits (0.8–2.4 V) |
| HV feedback control | 8 bits (0.8–2.4 V) |
| Slow-Control Communication, Digital and Analog Output | $I^2C$, LVDS and Analog buffer, respectively |

*Table* 2. **Specifications of CoCo chip**

| | |
|---|---|
| Pulse output frequency, kHz | $< 50$ (max.) |
| Pulse width, $\mu$s | $< 6.5$ (max.) |
| Power consumption, mW | $< 1$ |
| Supply voltage, technology | 3.3 V, 0.35 $\mu$ CMOS AMS |
| Current sense | 100 mV over 1.5 $\Omega$ |
| Opamp reference (internal), V | 1.2 |

can be adjusted via the CoCo ASIC to provide a gain of $10^6$ for the PMT in each case [5]. The specifications of both ASICs are presented in Tables 1 and 2.

*PROMiS — Analog Part Description.* The analog part of the PROMiS chip consists of a band gap, bias block, preamplifier, discriminator, analog buffer, and LVDS driver (Fig. 4). There are two 8-bit DACs: one to adjust the threshold level of the comparator and another to adjust the level of HV circuit. The preamplifier boosts the signal from the PMT. The comparator discriminates against a threshold level, which in turn specifies the Time Over Threshold (TOT, shown in Fig. 4). This pulse is sent on an LVDS line (0.4 m length) for digitization with an accuracy of $< 1$ ns and, finally, the digitized information is sent to shore for further processing. The band gap produces a stable 1.2 V reference, from which all the other bias voltages and currents in the bias block are derived. The preamplifier is a 2-stage charge amplifier (feedback: $R_f = 15$ k$\Omega$ k $C_f = 300$ fF), which is biased at 1 V. A single-stage comparator is designed to discriminate the output of the charge amplifier against the threshold value. The threshold voltage of the comparator can be set via $I^2C$. Conventional design is used for the LVDS circuit driving a 100 $\Omega$ kapton based transmission line, with common-mode feedback circuit. The CM voltage is set internally on chip to 1.2 V. To characterize the PMT and analyze the PMT signal, the preamplifier output is fed to an analog buffer.

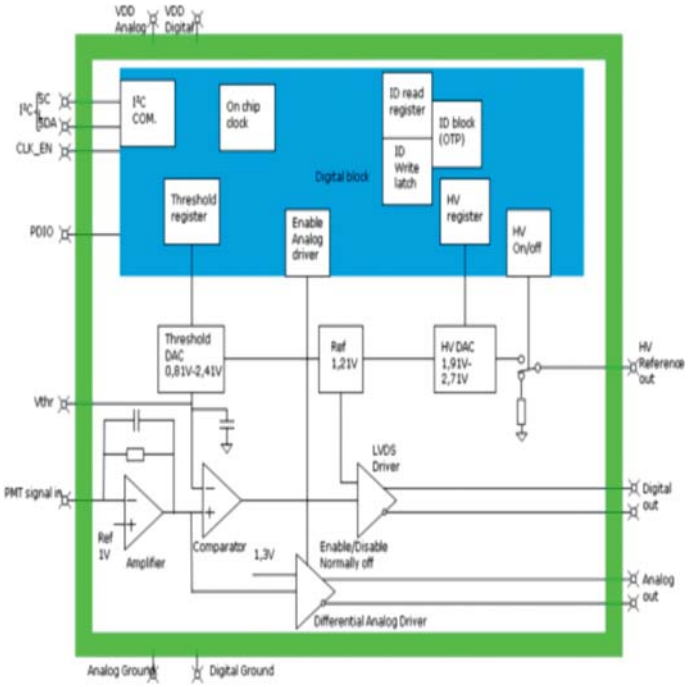


Fig. 4. Diagram of the PROMiS chip

*PROMiS —- Digital Part Description.* The digital part consists of a clock generator, a Power On Reset (POR), an $I^2C$ decoder, and an OTP (One-Time-Programmable) memory block with controller as is shown in the block diagram (Fig. 6). The clock generator generates a frequency of 10 MHz (30% variations due to process voltage and temperature). The accuracy of the clock is not very critical as it only samples a slow 250 kHz $I^2C$ SCL (clock) line. The $I^2C$ slave and the OTP controller was implemented using classical digital ASIC flow. Clock enable signal is provided to shut off the clock and save power. A facility to test the entire analog chain through $I^2C$ is provided. The HV circuit and analog buffer can be turned on/off using $I^2C$.

*CoCo Cockroft Walton Multiplier Feedback Control ASIC.* The PMT needs stable high voltage for its operation. The gain of the PMT is linear with the HV applied. The HV is generated using a CW multiplier circuit. An autotransformer with turns ratio of 12 is used to couple energy inductively from the 3.3 V supply to the CW circuit. The CW circuit has a high-resistive feedback circuit. The autotransformer is switched using an external switch. The ASIC supplies pulses to the switch controlling the autotransformer. The feedback of the CW circuit is

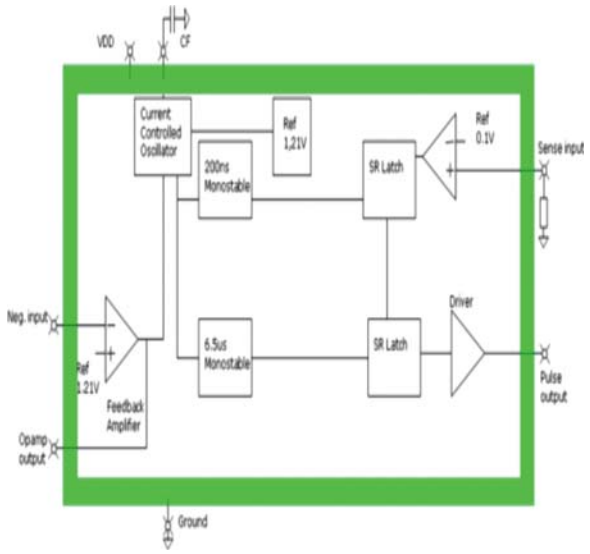


Fig. 5. Block diagram of the CoCo chip

controlled by the same ASIC. The pulses are of a definite width of 6.5 $\mu$s. The frequency of these pulses is controlled by the feedback of the HV circuit. The feedback voltage is converted to a current that is used to (dis)charge a capacitor. The magnitude of the current and the value of the external capacitor determine the frequency. The charging and discharging triangular wave across the capacitor is also used to generate internal clocks. On each rising edge of the clock, another pulse is generated with an on-time of 6.5 $\mu$s. For example, when the charge in the HV circuit is empty, the ASIC issues pulses at the highest frequency of 50 kHz. When the HV reaches the desired value (set by the HVDAC in PROMiS through $I^2C$), the frequency is reduced (around 200 Hz). The current sense input also helps to avoid the saturation of the autotransformer in case of a short circuit. Block diagram of CoCo chip is presented in Fig. 5.

## 2. THE OCTOPUS BOARD

Within each hemisphere, the LDVS signals from the PMT bases are collected on a custom electronics board (Fig. 6), called the Octopus Board, and transferred to the DOM Central Logic Board. The boards also provide connection for the electrical power to the PMT bases and the $I^2C$ communication control. For each PMT, the electrical power can be switched on/off individually by the slow control, and in case of overload of a PMT the power will be switched off automatically.

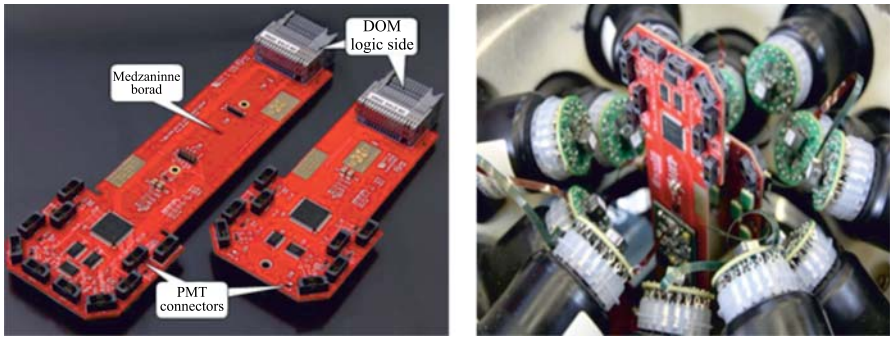


Fig. 6. Large and Short Octopus (left); detail of the Octopus inserted in the DOM (right)

This can be monitored by the Fault Flag (FFLG). A clock enabled signal to the PMTs for the $I^2C$ communication avoids digital interference.

**Functional Description.** The Octopus V4 Board acts as a hub inside the DOM. It merges all the PMT signal connections, controls the power supply, and redirects the $I^2C$ communication. On one side the Octopus V4 Board is connected to the PMTs and the piezo element. It distributes the power, clock enable and $I^2C$ communication to the PMTs and piezo element. It acts as an input for the differential signal from the PMTs and piezo element. On the other side the Octopus V4 Board is connected to the CLB. The power and the $I^2C$ bus are delivered from the CLB to the Octopus V4 Board. The differential signal is delivered to the CLB. The main functionalities of the board are listed bellow:

- to distribute and measure the 3V3 power;
- to distribute the 5V power;
- to multiplex the $I^2C$ channels;
- to control of the clock enable line;
- to transport the differential signals from the TDC channels and piezo;
- to provide an external Nreset signal.

## 3. POWER BOARD

For an efficient transfer of the electrical power, the voltage level must be high and the current low, because the power loss depends on the $I^2R$ of the cable. In addition, the different electronics of the DOM require many different voltage levels for their performance. Therefore, the power conversion board inside the DOM derives all different client voltage levels from an input voltage of 12 V. Modern converters at high frequency are used to obtain a high-efficient power conversion. To protect the other electronics inside the DOM from possible high-

frequency noise interference, the converter board is located in a shielded part of the cooling mushroom. On the other hand, cooling of the board will be more efficient at this location [6]. The PB is shown in Fig. 7.


Fig. 7. Picture of the first prototype of the DOM Power Board

The PB is attached to the CLB using three board-to-board connectors (J1, J2, J3). It receives power via J1 at nominal voltage of 12 V and produces six regulated power rails (1 V, 1.8 V, 2.5 V, 3.3 V, 3.3 V-PMT, 5 V) to power various electronic modules within the DOM via J2 and J3. It also provides a high voltage (from 0 to 30 V, 5 mA) programmable (via an $I^2C$ interface) voltage source for the nanobeacon module, via J1. Apart from the power rails, the PB has additional connections for $I^2C$ communication as well as remote sense and diagnostic signals.

## 4. CENTRAL LOGIC BOARD

The DOM Central Logic Board (CLB) is the main electronics board in the readout chain of KM3NeT. A picture of the CLB is shown in Fig. 8. The LDVS signals, generated by the PMT bases and collected and distributed by the Octopus Boards, arrive to the CLB where they are discretized by means of 1-ns resolution TDCs. The TDC data are sent on-shore after being organized and timestamped at the CLB. The CLB takes care also of the readout of several instruments, as it is the case of the compass, tiltmeter and temperature sensor, all of them integrated on the same CLB PCB, the piezo, the nanobeacon and the acoustic hydrophone. In order to synchronize the DOMs in KM3NeT, the CLB integrates the White Rabbit Protocol. It provides sub-nanosecond accuracy and picosecond precision of synchronization for large distributed systems (more than 1000 nodes over optical fibre and copper

Fig. 8. Picture of the DOM Central Logic Board

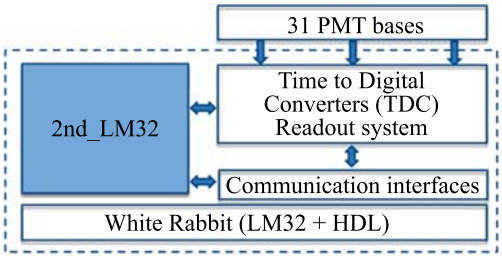


Fig. 9. Block diagram of the CLB firmware

lengths of up to 100 km). By using White Rabbit (WR), we are able to achieve precision time-tag measured data and trigger data taking in large installations and, at the same time, the same network can be used for data transmission [7]. The key technologies used are Synchronous Ethernet (SyncE) and Precision Time Protocol (PTP). The main component of the CLB is a Kintex FPGA. This device also allows the reconfiguration of the firmware of the CLB. It is feasible to store up to four FPGA images in a SPI memory, three of them reconfigurable. The non-reconfigurable one provides a safe start for the FPGA in case of corruption of the three reconfigurable images, being possible to choose to boot the FPGA with any of the four. Figure 6 shows the CLB board containing the FPGA where the readout and communication systems are implemented. The Kintex-7 FPGA is an FPGA family providing very low power consumption allowing a total CLB power consumption below 4 W. The control of the CLB is achieved through embedded software running in an LM32, an open source firmware microprocessor from Lattice. No operative system is used in order to reduce power consumption. The CLB contains two LM32 CPUs. One of them resides in the WR core which is dedicated to handle the PTP traffic and controlling the Phase Locked Loops (PLL) that are part of the timing system. The other CPU (2nd LM32) takes care of the slow control communication with the shore station. The block diagram of the CLB firmware is shown in Fig. 9.

## 5. TDC IMPLEMENTATION

The oversampling method uses a sampling frequency significantly higher than twice the bandwidth (or highest frequency) of the signal being sampled. For the KM3NeT readout system, the significantly higher sampling frequency is obtained using different edges of multiple phase-shifted clocks. This method is called “asynchronous oversampling” because the clocks used to create the sampling frequency are nominally equal to the data stream accuracy. High-speed phase-shifted clocks are generated from a slow system clock provided by a local clock oscillator placed on the CLB. A PLL inside the FPGA generates two clock phases

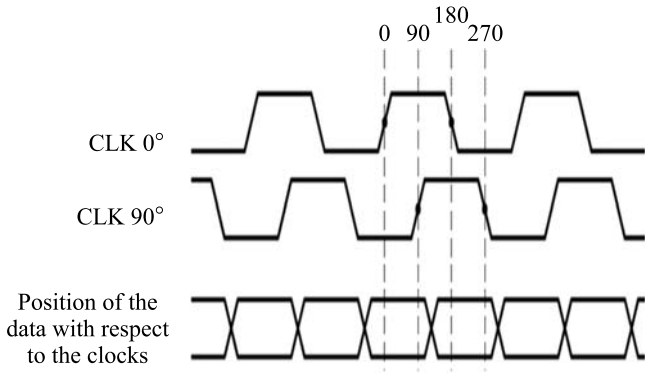


Fig. 10. Oversampling technique using two phase-shifted clocks

(CLK 0° and CLK 90°). These two phases are routed to a primitive deserializer, which is inside the input/output blocks of the FPGA. The generated CLK 0° and CLK 90° clocks make it possible to oversample an incoming data stream on four edges, increasing four times the sampling frequency. The function of the two extra clocks combination is shown in Fig. 10.

## 6. CLB READOUT FIRMWARE

TDC channels were designed in a Xilinx Kintex-7. Because of the programmable characteristic of an FPGA, a TDC readout implemented in this device has flexible characteristics. Here, a simplified TDC is designed to verify the idea of deserializing the raw data by means of dedicated input/output blocks of the FPGA. The CLB board includes a 25-MHz crystal oscillator; the clock signal is first transferred from a clock pin to a buffer in the centre of the FPGA and then fanned out to the inner PLLs to provide two high-frequency clocks of 250 MHz and 90° phase-shifted (see Fig. 11). 4-oversampling method increases the sampling frequency up to 1 GHz achieving the desired accuracy of 1 ns. The samples produced by deserializers are sent to specific blocks called Data Recovery Units (DRUs), where the data are reorganized and the digital pulse information is computed. The system readout generates an output of 48 bits where eight most significant bits are used to encode the PMT identifier, the next 32 bits indicate the time-stamp, and eight less significant bits are used to digitize the length of the pulse. In order to find tracks within the detector volume, the data are chopped in periods of time called frames or time-slices. Frames start at regular (programmable) intervals. Each frame is assigned a UTC time stamp and it is therefore uniquely identified. Data are related to the start of the frame using a relative offset provided by the Packet Transmission Unit (PTU). The CLB timing reference clock

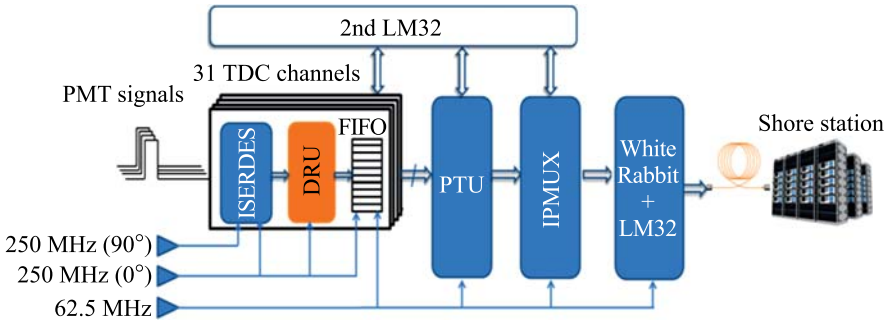


Fig. 11. Complete readout architecture

with a 1-ns phase precision and the UTC time are supplied by the White Rabbit PTP Core (WRPC) [8] that is implemented in the firmware. The CLB is connected to Ethernet via the 1000BASE-X MAC that is also incorporated in the WRPC. TDC data are transmitted to the shore via the endpoint of WRPC. This endpoint is basically a normal Ethernet MAC but it has time stamping capabilities allowing sub-nanosecond timing precision, such that it facilitates the PTP (IEEE588) protocol. The MAC is connected to an IP/UDP packet buffer stream selector (IPMUX). This IPMUX splits the data connecting to the MAC into separate streams, based on UDP port number. In the first place, the data need to be shipped from the DOM to the shore station, so IPMUX is mainly used as a UDP transmitted. Data that are received from the TDCs are stored in the Front-End FIFO memories where they are read by the PTU and passed to IPMUX. More functions have been integrated into the TDC firmware, such the high-rate veto function to avoid overloading the communication bandwidth and multihit function to process pulse widths larger than 255 ns. 31 TDC channels have been implemented, but the appropriate number of channels can be chosen according to the requirements of each DOM. The current implementation also offers a wide variety of interface options like an enable interface, which allows enabling or disabling remotely the TDC channels using the embedded software based on the LM32 microprocessor.

## 7. DOM POWER BUDGET

In Table 3, the power consumption breakdown of the DOM electronics is shown. The component with the highest power consumption is the CLB, with $2/3$ of the total power budget. The FPGA of the CLB and the SFP are the main power consumers.

*Table* 3. **DOM power budget**

| Board | Subcomponent | Power, W |
|---|---|---|
| Power Board | | 0.72 |
| Central Logic Board | | 4.715 |
| | FPGA (Kintex) | 2.25 |
| | SFP | 1.5 |
| | Clock conditioner | 0.5 |
| | Nanobeacon | 0.25 |
| | Temperature + humidity | 0.015 |
| | AHRS (tilt and compass) | 0.2 |
| Octopus Board Short | | 0.02078 |
| | OM $I^2C$ circuit | 0.02 |
| | OM $I^2C$ circuit | 0.00078 |
| Octopus Board Large | | 0.02078 |
| | OM $I^2C$ circuit | 0.02 |
| | OM $I^2C$ circuit | 0.00078 |
| PMT 31x | | 1.05 |
| | HV | 0.004 |
| | Detection | 0.03 |
| Digital piezo | | 0.5 |
| Total budget | | 7.03 |

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